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08EC021

M.Tech. Degree Examination, May/June 2010
CMOS VLSI Design

Time: 3 hrs. Max. Marks:100

Note: *1. Answer any FIVE full questions.*
2. Assume any missing data suitably.

1 a. Determine U_{out} for a CMOS inverter when the pull up P-MOS is in linear region. **(08 Marks)**
b. What is noise margin? Explain the same with suitable diagrams. **(06 Marks)**
c. For a nMOS FET, $V_T = 2V$, $t_{ox} = 0.1\ \mu m$, $M_n = 500\ cm^2/vs$, $W = L = 10\ \mu m$, $V_{gs} = 6V$, $V_{ds} = 1V$. Determine C_{ox} and drain current ($\epsilon_{ox} = 3.9$). **(06 Marks)**

2 a. Draw the different BICMOS circuits and discuss their behaviour. **(10 Marks)**
b. Describe twin well CMOS process. **(05 Marks)**
c. Draw the small signal MOSFET model and describe the different components. **(05 Marks)**

3 a. Define the terms sheet resistance, area capacitance, standard C_g and delay unit T. **(04 Marks)**
b. Derive an expression for the dimensions and the number of inverters needed to drive a large capacitive load C_L in a cascaded configuration. **(06 Marks)**
c. Describe metal interconnect and polycilicon / refractory metal interconnect associated with CMOS process enhancement. **(10 Marks)**

4 a. Describe λ - based rules for different types of contact cuts. **(08 Marks)**
b. Draw two input nMOS NAND gate and explain its behaviour. Derive expressions for V_{OL} and I_D. **(12 Marks)**

5 a. Draw circuit diagram and layout for CMOS NOR 2 and CMOS NAND 2 gates. **(08 Marks)**
b. Draw the circuit diagram and gate level schematic of CMOS SR latch based on NOR 2 case. Describe its operation and derive expression for switching times assuming suitable lumped capacitances using transient analysis. **(12 Marks)**

6 a. Describe circuit diagram and working of boot strap circuit. **(10 Marks)**
b. Derive the expression for V_{out} and A_v of a CS stage with resistive load. How can A_v be increased? What are the modifications for large R_D? **(10 Marks)**

7 a. Determine A_v for a differential pair and describe the vibration of drain current and overall trnasconductance through suitable plots. **(12 Marks)**
b. Explain the workers and main features of DOMINO CMOS structures with examples. **(08 Marks)**

8 Write short notes on :
a. Latch up in CMOS. **(05 Marks)**
b. Charge sharing. **(04 Marks)**
c. Checked storage elements. **(05 Marks)**
d. Pseudo nMOS inverter. **(06 Marks)**